Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-33. (Canceled)

34. (Currently Amended) A system for processing an input signal, the system comprising:

an adaptive predistortion subsystem for receiving said input signal and for producing a predistorted signal by applying a deliberate predistortion to said input signal, wherein said deliberate predistortion includes magnitude distortions which adjust a magnitude of said input signal; and

a signal processing subsystem receiving and processing said predistorted signal and producing a system output signal,

wherein

said adaptive predistortion subsystem distorts said Input signal to compensate for distortions in said system output signal;

said signal processing subsystem decomposes said predistorted signal into separate components, each of said separate components being processed separately;

said processing subsystem combines said components after processing to produce said system output signal; and

said deliberate predistortion applied to said input signal by said adaptive predistortion subsystem to produce said predistorted signal is adjusted based on said system output signal.

35. (Previously Presented) A system according to claim 34 wherein said signal processing subsystem comprises:

a signal decomposer for decomposing said predistorted signal into at least two components;

at least two signal component processor blocks, each signal processor block receiving an output of said signal decomposer and each signal processor block separately processes said output received from said signal decomposer; and

a combiner receiving a processed output from each of said at least two signal component processor blocks, said combiner producing said system output signal from said processed outputs

of said at least two signal component processor blocks.

36. (Previously Presented) A system according to claim 35 wherein at least one of said at least two signal component processor blocks includes an amplifier.

37. (Previously Presented) A system according to claim 36 wherein said amplifier is a non-linear amplifier.

38. (Previously Presented) A system according to claim 34 wherein said system is part of a signal transmission system.

39. (Previously Presented) A system according to claim 34 wherein at least some of said distortions are due to said combiner.

40. (Previously Presented) A system according to claim 36 wherein said amplifier is a switch mode amplifier.

41. (Previously Presented) A system according to claim 36 wherein said amplifier has a low output impedance.

42. (Canceled)

43. (Canceled)

44. (Previously Presented) A system according to claim 34 wherein said deliberate predistortion is based on at least one entry in a lookup table.

45. (Currently Amended) A method of processing an input signal to produce a system output signal, the method comprising:

a) receiving said input signal and accessing an entry in a lookup table;

b) applying a deliberate predistortion to said input signal to result in a predistorted signal, said deliberate predistortion being based on said entry;

c) decomposing said predistorted signal into at least two component signals;

d) combining said at least two component signals to produce said system output signal;

e) adjusting said deliberate predistortion based on said system output signal; and

f) updating at least one entry in said table.

46. (Previously Presented) A method according to claim 45 wherein said system output signal is an RF modulated version of said input signal.

47. (Previously Presented) A method according to claim 45 further including a processing step of separately processing each of said at least two component signals prior to step d).

48. (Previously Presented) A method according to claim 47 wherein said processing step includes amplifying at least one of said at least two component signals.

49. (Previously Presented) A method according to claim 47 wherein said processing step includes phase modulating at least one of said at least two component signals.

50. (Canceled)

51. (Previously Presented) A method according to claim 50 wherein said deliberate predistortion is based on an interpolation of entries in said table.

52. (Previously Presented) A system according to claim 34 wherein said predistortion subsystem receives a replica of said system output signal.

53. (Previously Presented) A system according to claim 35 wherein said deliberate predistortion is dependent on differences between said input signal and said replica of said system output signal.

54. (Previously Presented) A system according to claim 44 wherein entries in said lookup table are periodically updated based on characteristics of a replica of said system output signal.

55. (Previously Presented) A system according to claim 44 wherein said deliberate predistortion is based on an interpolation of entries in said table.

56. (Previously Presented) A system according to claim 34 wherein said predistortion subsystem includes:

determining means for determining said deliberate predistortion;

adjustment means for applying said deliberate predistortion to said input signal;

update means for periodically updating said determining means based on said system output signal.

57. (Previously Presented) A system according to claim 56 wherein said adjustment means receives parameters of said deliberate predistortion from said determining means.

58. (Previously Presented) A method according to claim 45 further including the step of taking a difference between said input signal and a replica of said system output signal to determine said characteristics of said system output signal.

59. (Canceled)

60. (Currently Amended) An adaptive predistortion subsystem for use with a signal processing system which produces a system output signal, the predistortion subsystem comprising:

determining means for determining a deliberate predistortion to be applied to an input signal, said determining means comprising

a lookup table having entries, said entries being used to determine said deliberate predistortion and

an interpolating means for determining values not found in said lookup table;

adjustment means for applying said deliberate predistortion to said input signal; and

update means for periodically updating said determining means based on characteristics of said system output signal.

61. (Previously Presented) An adaptive predistortion subsystem according to claim 60 wherein said adjustment means receives parameters of said deliberate predistortion from said determining means.

62. (Previously Presented) An adaptive predistortion subsystem according to claim 60 wherein said determining means comprises a lookup table having entries, said entries being used to determine said deliberate predistortion.

63. (Canceled)

64. (Previously Presented) An adaptive predistortion subsystem according to claim 60 wherein said deliberate predistortion is dependent on differences between said input signal and said replica of said system output signal.

65. (Previously Presented) A method according to claim 45 wherein said deliberate predistortion is at least partially based on characteristics of said system output signal.

66. (Previously Presented) A method according to claim 65 wherein said deliberate predistortion is determined in an iterative manner during transmission of said system output signal.

67. (Previously Presented) A system according to claim 34 wherein said predistorted signal is adjusted based on said system output signal and said input signal.

68. (Previously Presented) A method according to claim 45 wherein for step e), said deliberate predistortion is adjusted based on said system output signal and said input signal.

69. (Currently Amended) A system according to claim ~~34~~ 60 wherein said update means periodically updates said determining means based on said system output signal and said input signal.

70. (New) A system for processing an input signal, the system comprising:

an adaptive predistortion subsystem for receiving said input signal and for producing a predistorted signal by applying a deliberate predistortion to said input signal, wherein said deliberate predistortion includes phase distortions which adjust a phase of said input signal.; and

a signal processing subsystem receiving and processing said predistorted signal and producing a system output signal,

wherein

said adaptive predistortion subsystem distorts said Input signal to compensate for distortions in said system output signal;

said signal processing subsystem decomposes said predistorted signal into separate components, each of said separate components being processed separately;

said processing subsystem combines said components after processing to produce said system output signal; and

said deliberate predistortion applied to said input signal by said adaptive predistortion subsystem to produce said predistorted signal is adjusted based on said system output signal.

71. (New) A system according to claim 70 wherein said signal processing subsystem comprises:

a signal decomposer for decomposing said predistorted signal into at least two components;

at least two signal component processor blocks, each signal processor block receiving an output of said signal decomposer and each signal processor block separately processes said output received from said signal decomposer; and

a combiner receiving a processed output from each of said at least two signal component processor blocks, said combiner producing said system output signal from said processed outputs of said at least two signal component processor blocks.

72. (New) A system according to claim 71 wherein at least one of said at least two signal component processor blocks includes an amplifier.

73. (New) A system according to claim 72 wherein said amplifier is a non-linear amplifier.

74. (New) A system according to claim 70 wherein said system is part of a signal transmission system.

75. (New) A system according to claim 70 wherein at least some of said distortions are due to said combiner.

76. (New) A system according to claim 72 wherein said amplifier is a switch mode amplifier.

77. (New) A system according to claim 72 wherein said amplifier has a low output impedance.

78. (New) A system according to claim 70 wherein said deliberate predistortion is based on at least one entry in a lookup table.